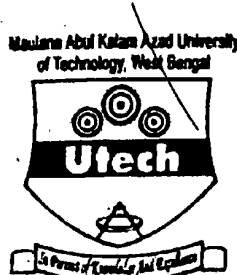


CS/BCA/EVEN/SEM-2/BCA-201/2016-17



**MAULANA ABUL KALAM AZAD UNIVERSITY OF  
TECHNOLOGY, WEST BENGAL**

**Paper Code : BCA-201**

**COMPUTER ARCHITECTURE & SYSTEMS  
SOFTWARE**

*Time Allotted : 3 Hours*

*Full Marks : 70*

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own  
words as far as practicable.*

**GROUP - A**

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for the following :

10 × 1 = 10

i) The 8085 instruction to transfer a data to a register  
in immediate mode is

a)  MOV

b) MVI

c)  LOAD

d) none of these.

ii) Memory address which refers to the successive  
memory words and the machine is called as

a) Word addressable

b) Bit addressable

c) Byte addressable

d) Terra byte addressable.

iii) What is true for a typical RISC architecture ?

- a) Micro-programmed control unit
- b) Instruction takes multiple clock cycles
- c) Have few registers in CPU
- d) Emphasis on optimizing instruction pipelines.

iv) The full form of PSW is

- a) program status word
- b) password status word
- c) program status work
- d) password status work.

v) In a virtual system, the addresses used by the programmer belong to

- a) Memory space
- b) Physical addresses
- c) Address space
- d) Main memory address.

vi) DMA stands for

- a) Digital Memory Address
- b) Direct Memory Access
- c) Digital memory Array
- d) Dual Memory Arithmetic.

vii) The transfer operation  $P : R_2 \leftarrow R_1$  will be executed only when

- a)  $P = 1$
- b)  $P = 0$
- c)  $P$  is 0 or 1
- d) None of these.

viii) The method updating the main memory as soon as a word is removed from the cache is called

- a) write-through
- b) write-back
- c) protected write
- d) cache-write.

ix) Stack overflow causes

- a) Hardware interrupt
- b) External interrupt
- c) Internal interrupt
- d) Software interrupt.

x) Data hazards occur when

- a) Greater performance loss
- b) Pipeline changes the order of read/write access to operands
- c) Some functional unit is not fully pipelined
- d) Machine size a limited.

**GROUP - B**

**( Short Answer Type Questions )**

Answer any *three* of the following.  $3 \times 5 = 15$

2. What is instruction cycle ? Compare and contrast hardwired vs micro-programmed control unit.  $2 + 3$

3. What do you mean by memory read and write operation ? Describe using register reference language.  $3 + 2$

4. Calculate the speed-up of a  $k$ -stage pipeline system processing  $n$  tasks.

5. a) What do you mean by "Micro-operation" ?

b) What are the different types of micro-operations ?  $2 + 3$

6. Write an Assembly level program to add two single byte numbers.

**GROUP - C**

**( Long Answer Type Questions )**

Answer any *three* of the following.  $3 \times 15 = 45$

7. a) With the help of a neat diagram show the structure of a typical arithmetic pipeline performing  $(A * B + C)$ .  $7$

b) What do you mean by Hazard ? State various types of hazards in brief.  $1 + 7$

8. a) What are cache misses ? Write down the techniques to minimize the cache misses. 2 + 6

b) A hierarchical main memory sub-system has the following specifications :

Cache access time : 50 ns

Main memory access time : 500 ns

80% of memory required for read

Hit ratio : 0.9 for read access and write through scheme is used.

(i) Calculate the average access time of the memory system considering only memory read cycle. 3

(ii) Calculate the average access time of memory system both for read and write cycle. 4

9. a) A computer has 512 kB cache memory and 2MB main memory. If the block size is 64 bytes then find subfield for

(i) associative memory

(ii) direct mapping

(iii) set-associative mapping. 10

b) How does cache memory increase the speed of processing? Explain. 5

10. a) Explain different types of addressing modes. 5

b) What are the advantages of Relative addressing mode over Direct addressing mode? 5

c) Differentiate between Vectored and Non-vectored interrupts. 5

11. a) Write a program to evaluate the arithmetic statement :

4 × 2

$$X = (A + B) / (C + D)$$

i) Using a stack organized computer with zero address operation instruction.

1024  
1024  
256  
x 2  
512 - 9  
1024 - 1

- ii) Using an accumulator type computer with one address instruction.
- iii) Using general register computer with two address instruction.
- iv) Using general register computer with three address instruction.

b) Write the features of 8085 micro-processor.

Discuss Flag Register in 8085.

4 + 3

