

MAULANA ABUL KALAM AZAD  
UNIVERSITY OF TECHNOLOGY,  
WEST BENGAL



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TECHNOLOGY, WEST BENGAL**

**Paper Code : BCA-201**

**COMPUTER ARCHITECTURE & SYSTEM SOFTWARE**

*Time Allotted: 3 Hours*

*Full Marks: 70*

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words  
as far as practicable.*

**Group - A**

**(Multiple Choice Type Questions)**

1. Choose the correct alternatives for the following:

1×10=10

(i) An exception condition in a computer system caused by an event external to the CPU is known as

(a) Halt

(b) Process

(c) Interrupt

(d) None of these

(ii) Cache memory is implemented using

(a) Dynamic RAM

(b) EEPROM SRAM

(c) EPROM

(d) ROM

(iii) The major objective in choosing page replacement policy is to

(a) minimize hit ratio

(b) reduce page size

(c) maximize hit ratio

(d) None of these

(iv) Whenever CPU detects an interrupt, what it do with current state?

(a) Save it

(b) Discard it

(c) Depends system to system

(d) First finish it

(v) The purpose of cache memory in a computer is to

(a) ensure fast booting

(b) reduce load on CPU registers

(c) replace static memory

(d) speed-up memory access

**Turn Over**

CS/BCA/EVEN/SEM-2/BCA-201/2017-18


- (vi) Where the result of an arithmetic and logical operation are stored?  
 (a) In Accumulator (b) In Cache Memory ~~X~~  
 (c) In ROM (d) In Instruction Registry ~~IR~~
- (vii) 8085 has a total of \_\_\_\_\_ registers.  
 (a) 10 (b) 11 ✓  
 (c) 12 (d) None of these
- (viii) The minimum time elapsed, between two read requests is  
 (a) Access time (b) Cycle time ✓  
 (c) Turnaround time (d) Waiting time
- (ix) The CPU activates the \_\_\_\_\_ output to inform the external DMA that the buses are in the high-impedance state.  
 (a) bus request (b) bus grant ✓  
 (c) cycle stealing (d) None of these ←
- (x) Which of the following bus is bi-directional?  
 (a) Address bus (b) Data bus ✓  
 (c) Control bus (d) Address-Data bus

## Group - B

(Short Answer Type Questions)

Answer any three questions.

5×3=15

2. Explain the Von-Neumann architecture with diagram. 
3. How the bus signal  $\overline{\text{MEMR}}$ ,  $\overline{\text{MEMW}}$ ,  $\overline{\text{IOR}}$  and  $\overline{\text{IOW}}$  are generated from 8085 microprocessor?
4. What are the uses of a System bus and Data bus? How do they differ from an Address bus?
5. Explain the role of program counter, stack pointer and address register.
6. Differentiate between direct addressing and indirect addressing with the help of a diagram.

## Group - C

(Long Answer Type Questions)

Answer any three questions.

15×3=45

7. (a) What are Hit ratio and Miss ratio in a memory system? 2
- (b) What do you mean by speed up ratio of a pipelining system? Explain with an example for 'k' segment pipeline.  $3+5=8$
- (c) Write a program to add two 8 bit number in assembly language. 5

8. What are the differences between RISC and CISC processors? Explain the concepts of sequential processing pipelining and parallel processing with example. What are the elements of a machine instruction? What is meant by memory access time? 4+6+3+2=15
9. (a) What is an instruction cycle? Draw the flowchart of an instruction cycle and explain with the help of timing diagram. 2+5=7
- (b) Change the following expression into Reverse Polish notation using stack implementation: 4  

$$Y = A * [B + (C * D)] / (E * F)$$
 Ans.  $CD * B + A * EF */$
- (c) Explain briefly the different types of Addressing mode. 4
10. Draw and explain a 4 bit arithmetic circuit which can perform the following: 15
- (a) ~~Add~~
- (b) Add with carry 001
- (c) Subtract with borrow
- (d) Subtract A+B+1
- (e) Transfer of A (Accumulator)
- (f) Transfer A (Accumulator)
- (g) Increment
- (h) Decrement
11. Write short notes of the following (any three): 5×3=15
- (a) DMA controller
- (b) Vector Processing
- (c) RISC and CISC
- (d) Virtual memory
- (e) Common bus system