MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : MCA-101

COMPUTER ORGANISATION & ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) In a stack computer, there is support for
      a) PUSH and POP instruction only
      b) Zero address instruction only
      c) Zero address instruction, PUSH and POP instruction
      d) None of these.

   ii) The purpose of cache memory in a computer is to
      a) Ensure fast booting
      b) Reduce load on CPU registers
      c) Replace static memory
      d) Speed up memory access.

iii) When signed numbers are used in binary arithmetic, then which one of the following terms would have unique representation for zero ?

a) Magnitude b) 1's complement
c) 2's complement d) None of these.

iv) How many address bits are required for a 1024 × 8 memory ?

a) 1024 b) 5
c) 10 d) None of these.

v) Instruction cycle is

a) Fetch-decode-execution
b) Decode-fetch-execution
c) Fetch-execution-decode
d) None of these.

vi) The 2's complement of 1101100 is

a) 0010100 b) 11001100
c) 11111111 d) 11110000.

vii) The full form of PSW is

a) Program Status Word
b) Password Status Word
c) Program Status Work
d) Password Status Work.

viii) The program that translates a high-level language program to binary is called

a) Byte code b) Operating system
c) Compiler d) None of these.

ix) 8085 is a ..... bit microprocessor.

a) 8 b) 16
c) 32 d) 64.

x) The data register are sometimes called

a) Source program b) Object program
c) Byte code d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw a NAND logic diagram that implements the following Boolean function :
   F (A, B, C, D) = ∑(0,1,2,3,4,8,9,12)
3. Design a full adder using two half adder and on OR gate.
4. Design a 2 - input XOR gate with minimum use of 2 - input NAND gate.
5. Why Grey code is called reflected code and Excess - 3 code is called self - complementing code ? What is the disadvantage of Grey code ? 2 + 2 + 1
6. Design a JK flip-flop using SR flip-flop.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Briefly discuss fixed - point number representation.
   b) A three level memory system having cache access time of 15 ns and disk access time of 80 ns has a cache hit ratio of 0.96 and main memory hit ratio of 0.9.
   What should be the main memory access time to achieve effective access time of 25 ns.
   c) What is DMA ? 5 + 5 + 5

8. a) What is Pipeline ? Describe about the performance of pipeline.

   b) Describe about Stack addressing mode, Register addressing mode, Direct addressing mode, Relative addressing mode. 2 + 5 + 8

9. a) Using the Booth's sequential multiplication method for unsigned number to Multiply + 14 and + 6.

   b) Explain the difference between three address, two address, one address and zero address instruction with a given expression : X = (A + B) * C

   c) What is op-code ? What is instruction code ? What is assembler ? 5 + 5 + (1 + 2 + 2)

10. a) Differentiate between CISC and RSC. What is Hardware control Design ?

    b) Describe about Pipeline hazards briefly. What is secondary memory ?

    c) Design and explain a 4 bit arithmetic unit circuit using 4 : 1 multiplexer which can perform the operations : add, add with carry, sub with borrow, sub, decrement, transfer A, increment. 3 + 2 + 3 + 2 + 5

11. Write short notes on any *three* of the following : 3 × 5

    a) Virtual Memory
    b) Instruction Pipeline
    c) Cache Memory
    d) Carry Look-ahead Adder (CLA)
    e) 4 : 1 Multiplexer.