



Name :

Roll No. :

Invigilator's Signature :

CS/MCA/SEM-1/MCA-101/2011-12
2011
COMPUTER ORGANIZATION AND
ARCHITECTURE

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$
 - i) The SOP form of logical expression is most suitable for designing logic circuits using only
 - a) XOR gates
 - b) NOR gates
 - c) NAND gates
 - d) OR gates.
 - ii) BCD subtraction is performed by using which complement representation ?
 - a) 1's
 - b) 2's
 - c) 10's
 - d) 9's.
 - iii) The r 's complement of number N_r is
 - a) $r - 1$'s complement + 1
 - b) $r^m - N$
 - c) both (a) & (b)
 - d) none of these.

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- iv) Floating point representation is the combination of
 - a) integer and fraction
 - b) mantissa and exponent
 - c) long integer and double
 - d) integer and double.
- v) What is the control unit's function in CPU ?
 - a) To transfer data to primary storage
 - b) To store program instruction
 - c) To perform logic operations
 - d) To decode program instruction.
- vi) When race condition occur in SR-flip-flop ?
 - a) S = 0, R = 0
 - b) S = 1, R = 0
 - c) S = 0, R = 1
 - d) S = 1, R = 1.
- vii) The gray code of decimal 7 is
 - a) 0111
 - b) 1011
 - c) 0100
 - d) 0101.
- viii) A demultiplexer has
 - a) one data input and a number of selection inputs, and they have several outputs
 - b) one input and one output
 - c) several inputs and several outputs
 - d) several inputs and one output.
- ix) The interrupt with highest priority in 8085 microprocessor is
 - a) INTR
 - b) TRAP
 - c) RST 7.5
 - d) RST 6.5.
- x) Gated D latch is called latch.
 - a) transparent
 - b) transport
 - c) traverse
 - d) nested.

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GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw the diagram of 3-bits Bi-directional shift register using mode control (*M*). When *M* is logic 0 then left shift and right shift for *M* is logic.
3. Differentiate between DRAM and SRAM organization.
4. a) What is truth table ? Why is it called so ?
 b) Why is NAND gate called universal logic gate ? 3 + 2
5. a) Simplify using K-map : $A'B'C + A'BC + AB'C + ABC$
 b) Write some disadvantages of K-map. 3 + 2
6. Design a 4 : 1 multiplexer using NAND gates.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Using K-map method minimize the following expression :

$$F (w, x, y, z) = m \Sigma (1, 5, 6, 12, 13, 14) + d \Sigma (2, 4)$$

 b) Implement XOR gate using NAND gate and NAND gate using NOR gate.
 c) Explain the difference between Ring and Johnson counter with proper state diagram and circuit diagram. 6 + (2 + 2) + 5

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8. a) What is Instruction Set ? Write down the program to compute $x = b * c + d/p$ using one address instruction. (2 + 4) + (2 + 4) + 3
- b) What is addressing mode ? Explain different types of addressing mode.
- c) Differentiate between micro programmed control unit and hardwired control unit. (2 + 4) + (2 + 4) + 3
9. a) Discuss the operation of 8085 microprocessor pins :
ALE, IO/M, HOLD, TRAP, INTR
- b) Describe Von Neuman architecture.
- c) What is microcontroller ? 6 + 6 + 3
10. a) Design a combinational circuit using different logic gates that can convert BCD code to its corresponding excess-3 code.
- b) What is DMA ?
- c) With the help of a diagram discuss how DMA transfer takes place. 6 + 3 + 6
11. Write short notes on any *three* of the following : 3 × 5
- a) DMA controller
- b) Polling vs daisy changing bus arbitration
- c) Floating point representation
- d) Cache memory
- e) Ripple counter.
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