2004

COMPUTER ORGANISATION AND ARCHITECTURE

Time Allotted: 3 hours *Full Marks: 70*

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer Question No.1 and any six from the rest

1 Answer any ten from the following: 1x10

i) Prove that, $(a + b'c')'.(ab' + abc) = 0$ in Boolean algebra.
ii) Why is a gated D latch called 'transparent' latch?
iii) Why demultiplexer is called data distributor?
iv) If A ⊕ B = C, then show that, A ⊕ C = B.
v) What is 'miss penalty'?
vi) "Synchronous counters can be used at higher frequency compared to an asynchronous counters having same MOD-number". Critically comment on the above statement.
vii) The Program Counter (PC) is called "memory pointer" – Justify your answer.
viii) What is universal shift register?
ix) What is the function of ALE in 8085 microprocessor?
x) The Q and Q' output of an edge triggered JK flip-flop are connected to its J and K inputs and clock is applied. Do you find any similarity with any well known flip-flop?
xi) "DMA is increasing the performance of CPU." – Justify .
xii) Can an input port and an output port have the same port address?
xiii) Express 9407 in BCD.
xiv) Express $(7652)_{10}$ in Excess-3 code.

2 a) Draw a NAND logic diagram that implements the following function 5

$$F(A, B, C, D) = \sum (0, 1, 2, 3, 4, 8, 9, 12).$$

b) Write down the differences between static RAM and dynamic RAM. 2

c) Explain the importance of accumulator in microprocessor. 3

3 a) Design a half adder circuit using minimum number of 2-input NOR gates only. Write down the truth table and Boolean functions also. 6

b) Determine the value of x, if $(211)_x = (152)_8$ 2

c) Subtract using 2's complement : 11001 – 1010 . 2

4. a) Show how a full adder can be converted to a full subtractor with the addition of just one inverter with the full adder circuit. 5
   b) Design a decimal to BCD encoder. 5

5. a) Convert a D flip-flop to a JK flip-flop. You can use additional circuiting if required. 5
   b) Design a 64K x 8 memory module using 16K x 1 memory chips. Draw the block diagram only. 5

6. a) Design a synchronous counter with JK flip-flop, which counts the following sequences: 0, 1, 2, 4, 5, 6 and again back to 0. 7
   b) What is the difference between memory mapped I/0 and I0-mapped I/0? 3

7. a) Explain Booth's multiplication algorithm with a suitable example. 8
   b) What is the difference between hardware interrupt and software interrupt? 2

8. a) Design a BCD ripple counter and explain its operation with timing diagram. 7
   b) How the same buses are worked together as low order address bus and data bus in 8085 microprocessor? 3

9. a) How DMA is initiated and how DMA controller works? 7
   b) What is instruction cycle? What are the different phases of instruction cycle? 3

10. a) Evaluate the following arithmetic expression using single accumulator organisation instruction and stack organization instruction. 6

    $X = A - B + C * (D/E)$

    b) How the effective address is calculated in direct address mode and an indirect address mode? 4

11. Write short notes on <u>any two</u> of the following: 5x2
    (a) Interrupt lines of 8085 microprocessor.
    (b) Vector processing.
    (c) Von – Neumann architecture.
    (d) Addressing modes.

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