ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2006

COMPUTER ORGANIZATION AND ARCHITECTURE

SEMESTER - 1

Time : 3 Hours] [Full Marks : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. *1* and any *four* from the rest.

1. Answer any *five* from the following : 5 × 2 = 10

   i) What are the different flags in 8085 microprocessor ?

   ii) Why is multiplexer called "data selector" ?

   iii) What is cache memory ?

   iv) Add the following numbers using 2's complement method :

   + 49 and – 37.

   v) What is meant by Harvard Architecture ?

   vi) What is the purpose of stack in microprocessor ?

   vii) Define *T* state, machine cycle and instruction cycle.

   viii) What is hit ratio and miss penalty ?

2. a) $f(A, B, C, D) = \sum m(0, 2, 3, 5, 6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14, 15)$.

   Realize the minimised function using only NAND gates.

   b) A digital computer has a common bus system for *K* registers, each of *n* bit capacity. The bus is constructed with multiplexers.

      i) What size of multiplexers is needed ?

      ii) How many multiplexers are there in the bus ?

   c) Draw a comparison between RISC and CISC machines. 5 + 5 + 5 = 15

3. a) Give the block diagram of 8085 microprocessor clearly mentioning different functional units.

   b) Draw the timing diagram of the OPCODE fetch machine cycle.

   c) Explain the function of the ALE signal in 8085 microprocessor.

   d) What is the duration of a *T*-state in 8085 microprocessor ? 6 + 6 + 2 + 1

4. a) Show how a full adder can be converted to a full subtractor with the addition of just one inverter with the full adder circuit.

   b) Design a decimal to BCD encoder. 8 + 7

5. a) Design a BCD ripple counter and explain its operation with timing diagram.

   b) Explain Booth's multiplication algorithm with suitable example. 8 + 7

6. a) With a suitable diagram explain the concept of microprogramming.

   b) What are the different stages of instruction pipelining ?

   c) Define Speedup, Efficiency and Throughput of a pipeline.

   d) What is pipeline staling ? 7 + 2 + 4 + 2

7. a) What is the difference between a latch and edge triggered flip-flop ?

   b) Draw the circuit diagram of a master-slave JK flip-flop using all NAND gates and explain the circuit operation.

   c) Convert a D flip-flop to a JK flip-flop using additional gates. 3 + 7 + 5

8. Write short notes on any *three* of the following : $3 \times 5 = 15$

   a) DMA

   b) Vector Processing

   c) Interrupt lines in 8085 microprocessor

   d) von Neumann architecture

   e) Virtual memory.