ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2009

COMPUTER ORGANIZATION & ARCHITECTURE

SEMESTER - 1

Time : 3 Hours] [Full Marks : 70

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) 1 nibble is equal to

a) 4 bits b) 8 bits

c) 12 bits d) 16 bits.

ii) 364 (8) = ... (10)

a) 222 b) 102

c) 244 d) 230.

iii) 6B9 (Hexadecimal) = ... (Binary)

a) 11010111001 b) 01010111010

c) 11110011001 d) 101010101010.

iv) Value of $(a + b'c')' . (ab' + abc)$ = ...

a) zero b) one

c) a d) ab.

v) Inter-record gap is related to which one of the following storage devices ?

a) Floppy Disk b) Hard Disk

c) CD-ROM d) Magnetic Tape.

vi) Which of the following registers holds an instructon until it is decoded ?

a) Index Register b) Memory Address Register

c) Instruction Register d) Data Register.

vii) Gated *D* latch is called ..... latch.

a) Transport latch b) Traverse latch

c) Transparent latch d) Nested latch.

viii) For bulk storage, which one of the following storage devices is most suitable compared to others in respect to cost ?

a) Hard Disk b) Magnetic Tape

c) CD-ROM d) DVD.

ix) INTR is an interrupt signal of ..... priority.

a) highest b) lowest

c) medium d) same.

x) Which one of the following operations is not performed by ALU ?

a) Clear b) Floating point calculation

c) Logical OR d) Logical AND.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Design a half adder circuit using minimum number of 2-input NOR gates only. Write down the truth table and Boolean function also.

3. Convert a JK flip-flop to a D flip-flop. You can use additional circuitry, if required.

4. Construct a 5×32 decoder with the help of 2×4 decoders. Show the block diagram only.

5. Write short notes on any *one* of the following :

   i) Universal gate

   ii) Master-Slave JK flip-flop

   iii) Cache Memory.

6. Obtain the POS form of $F (A, B, C, D) = AB\bar{C} + A\bar{D} + CD$.

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. a) Prove that $(a + b' + c')' . (ab' + abc) = 0$ in Boolean algebra.

   b) Why does 11 come before 10 in the Karnaugh map ?

   c) How many input line(s) and selection line(s) must be present in a demultiplexer that has 32 possible output lines ?

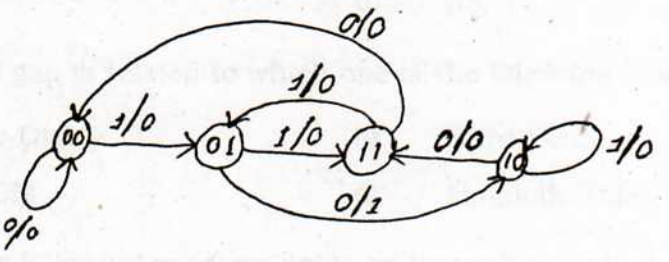
   d) Why is a gated D latch called 'transparent' latch ?

   e) Design a combinational circuit using different logic gates that can convert BCD code to its corresponding Excess-3 code. $2 + 2 + 1 + 2 + 8 = 15$

8. What is pipeline architecture ? What is speed-up, efficiency and throughput of a pipe-lined architecture with reference to non-pipelined architecture. What is locality of reference ? Write down the various ways in addressing cache. Write down the difference between direct, indirect and implicit address instructions.

   $2 + 3 + 2 + 5 + 3 = 15$

9. a) Design a sequential circuit using JK flip-flop which realizes the following scale diagram :



   b) Draw a schematic diagram of Master-Slave JK flip-flop.

   c) Find out the Q value of R if $(125)_R = (203)_5$. $8 + 4 + 3 = 15$

10. a) Show how two 4 : 1 MUX can be connected to provide an 8 : 1 MUX.

b) Design a mod 8 synchronous counter.

c) What is vector processing ? 5 + 5 + 5 = 15

11. a) Design 16 × 4 bit RAM using 4 × 2 bit RAM IC modules.

b) What is the difference between memory mapped I/O and I/O mapped I/O ?

c) Briefly explain arithmetic & logic instructions. 6 + 4 + 5 = 15

12. Write short notes on any *three* of the following : 3 × 5 = 15

a) Self-complementing property of Excess-3 code

b) DMA controller

c) von Neumann architecture

d) Addressing modes.

END