Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/MCA/SEM-1/MCA-101/2009-10

2009
COMPUTER ORGANIZATION AND ARCHITECTURE

Time Allotted : 3 Hours | Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) The r's complement of number N_r is

      a) r – 1's complement + 1

      b) $r^m - N$

      c) both (a) & (b) are true

      d) both (a) & (b) are false.

   ii) The general rule for converting a number $N_r (N_m \ldots N_2 N_1)$ with m number of digit into binary is

      a) $\sum_{i=0}^{m-1} r^i N_i$ b) $\sum_{i=1}^{m} r^i N_i$

      c) $\sum_{i=0}^{m} r^i N_i$ d) none of these.

iii) The interrupt with highest priority in 8085 microprocessor is

a) TRAP b) RST 7·5

c) INTR d) RST 6·5.

iv) Control unit of a processor is basically

a) MUX b) DEMUX

c) Decoder d) Encoder.

v) Multiplexer is combinational circuit which gives

a) several output

b) no output

c) 3 output

d) 1 output.

vi) $(1 + xy + x\breve{y} + yz + xz)$ is equal to

a) $x\breve{y} + yz$ b) xyz

c) 0 d) 1.

vii) Load store architecture followed in

a) Harvard architecture

b) Von Neumann architecture

c) both (a) & (b)

d) none of these.

viii) In which addressing mode, the effective address of the operand is generated by adding a constant value to the contents of a register ?

a) indirect mode

b) index mode

c) absolute mode

d) direct mode.

ix) 'CALL' instruction containing *T* state of the opcode fetch comprised of

a) 6 *T* state

b) 4 *T* state

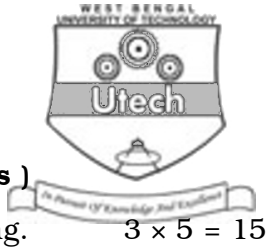
c) 18 *T* state

d) none of these.

x) To design MOD 10 up/down counter the no. of flip-flop requirement is

a) 4 b) 8

c) 10 d) 16.



GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What do you mean by instruction cycle, machine cycle and *T* states ? 5

3. a) Convert $(B6C7)_{16}$ to decimal.

   b) Write the differences of 1's complement and 2's complement representations of the binary number system. 2 + 3

4. a) Draw the block diagram, Boolean expression, logic symbol and truth table of X-OR gate.

   b) Show how a two input X-OR gate can be constructed only from 2 input NAND gate. 3 + 2

5. Derive a circuit using the following function :

   $F(x, y, z) = \Sigma(0, 1, 5, 7) + d(2)$.

   What is the disadvantage of *k*-map ? 4 + 1

6. Why Grey code is called self-reflective code and Excess-3 code is called self-complementing code ? What are the problems with Grey code ? 3 + 2

7. Evaluate the following arithmetic statement using three addresses and one address instructions :

$X = (A + B) * (C + D)$. 5

GROUP – C
(Long Answer Type Questions)
Answer any *three* of the following. 3 × 15 = 45

8. a) Write an algebraic expression for the given functions and simplify algebrically.

$F = (x, y, z) = \pi (0, 1, 4, 5)$

b) Simplify algebraically :

$$\left[X^{l}\left(Y^{l}+Z^{l}\right)\left(X+Y+Z^{l}\right)\right]$$

c) Prove that a full subtractor can be constructed using two half-adder and an additional external circuit.

d) Construct a one-bit BCD adder using two 4-bit binary adder and additional external circuit. 3 + 3 + 3 + 6

9. a) Explain the need of Cache Memory in computer.

   b) What do you understand by Cache Coherence ? How is it overcome ?

   c) Explain the Associative Cache Mapping technique.

   d) What are the advantages of Set Associative Cache mapping over the Direct Cache Mapping ?

   2 + (2 + 3) + 4 + 4

10. a) What do you mean by priority interrupt ? Describe the priority scheme in 8085 microprocessor.

   b) Describe chain priority interrupt.

   c) What are the differences between Memory Mapped I/O and I/O mapped I/O ? 5 + 5 + 5

11. a) What is DMA ?

   b) With the help of a diagram discuss how DMA transfer takes place.

   c) Differentiate between hardwared control unit and micro-programmed control unit. 2 + 8 + 5

12. Write short notes on any *three* of the following : 3 × 15

a) Virtual Memory

b) Booth's Algorithm for Multiplication

c) Floating point representation

d) Von Neumann *vs* Harvard architecture

e) Arithmetic Logic Unit (ALU).